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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/821,983 | 04/12/2004 | Toshio Mukunoki | 60188-837 | 2084 |

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| EXAMINER | |
|---|---|
| WENDLER, ERIC J | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2824 | |

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/821,983 | MUKUNOKI ET AL. | |
| | Examiner | Art Unit | |
| | Eric Wendler | 2824 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *4/12/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 8-16* is/are rejected.

7)☒ Claim(s) *3-7 and 17-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search History*.

## DETAILED ACTION

1. This action is responsive to the following communications: the Application and Information Disclosure Statements filed on April 12, 2004.

2. Claims 1-20 are pending in the case. Claims 1 and 2 are independent claims.

### *Priority*

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. JP 2003-112576, filed on April 17, 2003.

### *Claim Objections*

4. **Claims 17 and 19 are objected to under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.** The examiner has interpreted these claims in light of the specification as meaning that both the first and second memory cells are comprised of the same members as the first and second memory cells of the previous embodiments (paragraph 0167 of the present application). Appropriate correction of these claims is required.

### *Claim Rejections - 35 USC § 102*

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

**6. Claims 1-2, 12, and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by the US Patent to Hidaka (6,646,911).**

7. **Regarding claim 1,** Hidaka teaches, in Fig. 1, a plurality of first memory cells arranged in a matrix (**10**), and control lines **BL*n*** and **WL*n*** connecting a subset of the plurality of first memory cells which are aligned in a row direction or a column direction. He also teaches second memory cells connected to the control lines wherein the second memory cell is configured to allow a higher stress to be passed though it for testing purposes (column 5, lines 19-36; column 25, lines 27-34; column 26, lines 8-18, 66-67; column 27, lines 1-25). It is implicitly drawn from this teaching that if the same stress voltage is applied to both the normal memory cell and the dummy cell, the dummy cell will retain data.

8. **Regarding claim 2,** Hidaka teaches a semiconductor memory device comprising a plurality of first memory cells arranged in matrix; a plurality of word lines each connecting a subset of the plurality of first memory cells which are aligned in a row direction; a plurality of bit lines each connecting a subset of the plurality of first memory cells which are aligned in a column direction; and a plurality of second memory cells which are connected to at least either of the word lines and the bit lines, wherein the first memory cells and the second memory cells each have a charge storage portion for storing charges, and when voltage application to the word lines or the bit lines changes the amounts of charges stored in the charge storage portions of the first memory cells and the second memory cells, the amount of change in charges in the second memory

cell is larger than the amount of change in charges in the first memory cell (column 5, lines 19-36; column 25, lines 27-34; column 26, lines 8-18, 66-67; column 27, lines 1-25).

9. **Regarding claim 12,** Hidaka teaches the plurality of second memory cells are arranged with two or more being connected in series on each of the bit and/or word lines (column 5, lines 25-28).

10. **Regarding claim 14,** Hidaka teaches the plurality of MJT cells are arranged so that the tunnel currents can pass through them in parallel during the burn-in test, which is the effect that parallel connection with the word and bit lines would have (column 18, lines 4-12, 63-67; column 19, lines 1-3). It is implicitly drawn that the dummy cells have this same effect of parallel connection when the burn-in test is performed on them.

***Claim Rejections - 35 USC § 103***

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**12. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hidaka in view of the US Patent to Ferris et al (5,268,869).**

13. **Regarding claims 8-9,** Hidaka teaches all the claims elements as discussed above but fails to teach a switch means or fuse element for separating electrical connections between the word lines and or the bit lines and the second memory cells. Ferris teaches, in Fig. 5, dummy cells that are attached to a dummy word line and can

be separated from such by blowing a fuse (column 4, lines 51-64; column 6, lines 19-22). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine the teachings of Hidaka with the teachings of Ferris to get a method of separating the dummy cells from the regular array to improve reliability.

**14. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hidaka, Ferris et al, and the US Patent Application Publication of Kuge et al (US 2004/0145959).**

15. **Regarding claims 10-11,** Hidaka and Ferris teach all the claimed elements as discussed above, but fail to teach where the switch means is an MIS transistor and a memory cell stores information that controls the MIS transistor. Kuge teaches, in Fig. 4, an MIS transistor **$NQ_6$** that acts as a switch to short-circuit a bit line to a complement bit line, and a memory block that contains a circuit BEQR that stores information on the whether to turn the MIS transistor on or off. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine the teachings of Hidaka and Ferris with the teachings of Kuge to get another method of separating the dummy cells from the regular array to improve reliability.

**16. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hidaka in view of the US Patent Application Publication of Kuge et al (US 2004/0145959).**

17. **Regarding claim 13,** Hidaka teaches all the claimed elements but fails to teach an equalization circuit that equalizes pieces of data stored in the second memory cells and supplies an equalization result. Kuge teaches equalization circuits BEQR and

BEQL contained in memory blocks MBKR and MBKL that equalize the data from memory cells MCR and MCL (paragraphs 0061-0064). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine the teachings of Hidaka with the teachings of Kuge for the purpose of measuring the stress applied to the bit lines and equalizing the data to be conveyed to the rest of the circuit.

**18. Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hidaka in view of the US Patent to Nishimoto et al (6,444,514).**

19. **Regarding claims 14-15,** Hidaka teaches all the claimed elements but fails to teach that the second memory cells are connected in parallel to word and/or bit lines, and switching transistors for controlling the connections between the memory cells and these lines. Nishimoto teaches, in Fig. 2, memory cells **M** that are connected in parallel to word and/or bit lines, with switching transistors **SWMOS1** and **SWMOS2** controlling the connections between the memory cells and the word and bit lines (column 9, lines 54-67; column 10, lines 1-2). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine the teachings of Hidaka with the teachings of Nishimoto for the purpose of being able to select the proper lines and cells.

**20. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hidaka in view of the US Patent to Hashimoto (5,408,433).**

21. **Regarding claim 16,** Hidaka teaches all the claimed elements but fails to teach verification circuits for determining whether or not a writing operation or an erasing operation is normally performed on the memory cells. Hashimoto teaches a reference circuit that determines whether a memory cell is in a written condition or an erasing

condition (column 4, lines 18-26). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine the teachings of Hidaka with the teachings of Hashimoto for the purpose of verifying whether the cell was written to or erased and assigning a "0" or "1" accordingly.

***Allowable Subject Matter***

22. **Claims 3-7, and 17-20 are objected to** as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

23. **Regarding claims 3-7,** the prior art fails to teach first and second memory cells that differ in the composition or shape of the tunnel or capacitor insulating films, and the floating and control gate electrodes, wherein the capacitor insulating films of the second memory cells have a lower resistivity that those of the first memory cells, and are formed as a stacked film containing silicon oxide and nitride films, wherein the floating gate electrodes of the first memory cells have a smooth upper surface, and the floating gate electrodes of the second memory cells have a surface with projections and depressions, and wherein the ratio of the area in which the floating and control gate electrodes face each other with the capacitor insulating film in between for the second memory cells is larger that the first memory cells.

24. **Regarding claims 17-20,** the prior art fails to teach first and second memory cells formed of the same members as those of claim 3 that are connected to source electrodes by separate source lines, and wherein second memory cells connected in

serial includes cells that are both shaped identically and differently from the first memory cells.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Wendler whose telephone number is (571) 272-5063. The examiner can normally be reached on Monday - Friday 8AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EJW
11/23/05

VAN THU NGUYEN
PRIMARY EXAMINER